CLAIMS

What is claimed is:

1. A method for recovering a clock from a data input sequence, comprising:

sampling, according to a sampling clock, the input sequence such that a first set of samples corresponds to data values and a second set of samples corresponds to edges between the data values;

determining phase error between data transitions in the input sequence and the sampling clock phase, based on amplitudes of the sampled edges; and

adjusting the sampling clock's phase based on the determined phase error.

2. The method of Claim 1, wherein the phase error is proportional to an amplitude of a sampled edge.

3. The method of Claim 1, further comprising:

adding/subtracting sampled edge amplitude values to form an error value, according to a direction of each transition about each edge, wherein an amount of phase error is indicated by the error value.

4. The method of Claim 3, further comprising:

ignoring a sampled edge at which no transition occurs.

5. A phase detector, comprising:

a sampling clock generator which generates a clock at an oversampling rate compared to a data rate of an input sequence;

a first samplers which samples data values of the input sequence;

a second sampler which samples edges between the data values; and

a data phase detector which determines phase error between data transitions in the input sequence and the sampling clock phases, based on amplitudes of the sampled edges, the determined phase error being fed into the sampling clock generator to adjust the phase of the sampling clock.

6. The phase detector of Claim 5, wherein the phase error is proportional to an amplitude of a sampled edge.

7. The phase detector of Claim 5, wherein the phase detector comprises:

switches for adjusting polarities of sampled edges based on previous and next data values, the polarity-adjusted sampled edges being added together to form a phase error indication, the phase error indication driving the sampling clock generator.

8. The phase detector of Claim 7, wherein any of said switches ignores a sampled edge if no transition occurs between the previous and next data values.

9. The phase detector of Claim 7, wherein the data phase detector comprises plural voltage-to-current converters which convert sampled edge voltages to currents, such that the switches switch current polarities, and wherein the sampled edge currents are added together via hard-wiring.

10. A phase detector for recovering a clock from a data input sequence, comprising:

means for sampling, according to a sampling clock, the input sequence such that a first set of samples corresponds to data values and a second set of samples corresponds to edges between the data values;

means for determining phase error between data transitions in the input sequence and the sampling clock, based on amplitudes of the sampled edges; and

means for adjusting the sampling clock's phase based on the determined phase error.